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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,332	11/04/2003	Ghasi R. Agrawal	03-1343	5874

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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/701,332	AGRAWAL ET AL.	
	Examiner	Art Unit	
	STEVE NGUYEN	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-17,19-23,25 and 26* is/are pending in the application.

4a) Of the above claim(s) ____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-17,19-23,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 15-17, 19-23, 25, and 26 are currently pending.

Response to Arguments

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

Applicant's argument that Tanishima does not disclose faking defects is not found persuasive. Tanishima details the process of faking defects to remap good elements with redundant elements in the discussion of Fig. 3. Fuses FS0-FSn are fuses that are responsible for mapping faulty memory locations to corresponding redundant locations RM/LA0-RM/LAn as is conventional in the art. Tanaka provides for testing of the redundant memory even if it is not used by faking defects to temporarily map the redundant elements (col. 7, lines 34-37; test data is fed as the failed portion instead of actual fail data being fed). This is done by temporarily bypassing the fuses to remap the redundant elements through switch SW2 (col. 7, lines 37-42) such that the redundant memory is remapped even if not required (col. 7, lines 48-55; it is clear that the redundant memory is not required because the fuse element need not be written to).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 15-17, 19-23, and 25-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Frankowsky (US Pat. 6,961,880) in view of Miller et al (US Pat. Pub. 2003/0237061; hereinafter referred to as Miller) in view of Shih et al (US Pat. 6,661,719; hereinafter referred to as Shih) in view of Tanishima et al (US Pat. 6,999,357; hereinafter referred to as Tabishima).

As per claims 15 and 21:

Frankowsky teaches a method for testing memory, said method comprising:

- performing a first test, wherein functional memory is tested (Fig. 2, 22; col. 2, lines 49-51);
- repairing the functional memory by adding access to redundant elements, thereby providing repaired functional memory (Fig. 2, 24; col. 2, lines 51-52);

- after repairing the functional memory, adding access to redundant memory not required for the repair of the functional memory (col. 2, line 63 to col. 3, line 1; the unused redundant memory is accessed and tested in step 28 of Fig. 2 which occurs after steps 22 and 24); and
- performing a third test, wherein redundant memory is tested (col. 2, lines 59-63).

Not explicitly disclosed by Frankowsky is wherein the step of adding access to redundant memory which is not required for the repair comprises faking defects to remap good elements with redundant elements. However, Tanishima in an analogous art teaches a method of adding access to redundant memory which is not required by faking defects to remap good elements with redundant elements (col. 7, lines 34-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the method of Tanishima for adding access to redundant memory which is not required. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing do would have enabled one to perform testing on the redundant memories without actual replacement with the redundant memory cell array (Tanishima; col. 8, lines 5-8).

Not explicitly disclosed by Frankowsky or Tanishima is performing a second test, wherein the repaired functional memory is tested. However, Miller in an analogous art teaches re-testing the functional memory which has been repaired (Fig. 1; 16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to re-testing the functional memory which has been repaired.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing so would have ensured that the repair was effective (Miller; paragraph 5).

Not explicitly disclosed by Frankowsky, Tanishima, or Miller is after testing the repaired functional memory and than adding access to redundant memory not required for repair of the functional memory, performing a third test, wherein redundant memory is tested. However, Shih in an analogous art teaches repeating burn-in testing of redundant memory (Fig. 3; 160). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to repeat the burn-in step 28 in Frankowsky after the repair step 30. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that repeating the burn-in sequence would have forced each memory cell to switch with the burn-in level many times further exposing faulty memory arrays (col. 5, lines 12-15).

As per claims 16 and 22:

Frankowsky further teaches using repair information to repair the functional memory (col. 2, lines 51-54).

As per claims 17, 19, 23, 25:

Frankowsky and Miller substantially teach the testing mode and method as detailed above. However, not explicitly disclosed is forcing usage of redundant elements which are not needed to be used for repairing the memory; and checking interaction between redundant elements.

However, Tanishima in an analogous art teaches forcing usage of redundant elements which are not needed to be used for repairing the memory; and faking defects to remap good elements with redundant elements (col. 6, lines 30-44 and col. 7, line 66 to col. 8, line 8). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to force usage of redundant elements which are not needed to be used for repairing the memory. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that doing do would have enabled one to perform testing on the redundant memories without actual replacement with the redundant memory cell array (Tanishima; col. 8, lines 5-8).

As per claims 20 and 26:

Frankowsky further teaches wherein the step of adding access to redundant memory not required for repair of the functional memory comprises adding access to all remaining redundant memory, and wherein the step of performing a third test comprises testing all the remaining redundant memory (col. 2, line 65 to col. 3, line 1; Frankowsky teaches accessing and testing all unused redundant elements).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEVE NGUYEN whose telephone number is (571)272-7214. The examiner can normally be reached on M-F, 10am-6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Ellis can be reached on (571) 272-4205. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steve Nguyen
Examiner
Art Unit 2117

/Kevin L Ellis/
Supervisory Patent Examiner, Art Unit 2117